



B75H2-M2

Rev :1.0

ECS CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/11/09	Change from H67H2-M3: 1. Del PCI SLOT *2&Add PCIeX1 slot *2 2. Del PCI Bridge IT8893CX 3. Add TPM/LPT/LPC DEBUG HEADER 4. Super IO change to IT8728CX 5. Chipset change to H61
V.1.0	2010/12/06	Change from H61H2-M5:VA 1.P23 change 5V_CTRL FOR EZ_CHANGE 2.P24 CHANGE Cg FOR COLAY VIA 1705CE 2010/12/06 FQ 3.P23 ADD VIN2 VIN5 VIN6 20101208 ADD FOR RESERVE 2010/12/09 4.P25 change front line damping resistor 75ohm to 16ohm when in stall VIA codec 5. P13 Add 4PIN SYSFAN2 1211 FQ Change 12V EC, MC110/MC111 10U-16VY-12 6. P22 Change SATA1/2 footprint 90 7. P23 PCH_THRM_L NO connect ,PULL HIGH VCC3 8. P28 USB3 USE NEC720200 9. P9/P10 PWM RT8859MGQW + RT9612BGS SUS RT8859AGQW + RT9619APS 10.P21/22 Change USBX4 TO USBX2 PS2 Change TO PSUSB 1213 11. P13 CHANGE 4PIN SYS&PWR FAN TO 3PIN FAN
V.2.0	2011/01/18	Change from H61H2-M5 V 1.0: 1. Del HDMI CONNECT (P21) 2. DEL LPT HEADER, 3. change P23 I/O BC230 TO 1U-06 ,ADD P13 C70,C71 4. Change Audio chip to ALC892 COY-LAY ALC662
V.5.0	2011/08/30	Change from H61H2-M5 V 2.0: 1.P28 Del NEC 720200(2 Ports) and then add NEC 720201(4 Ports) 2.P22 Add USBVCC4 for USB3F 3.P26 Del TPM and then Add LPC for Debug card 4.P27 Change the pin of Data Singal 5.P23 Change VBAT_IO to VBAT_IO_S for avoid starting up after closing illegally; reduce inrush current MC120 1u-06-->2.2u-06 6.Thermistor resistor footprint change to 0402(RT1,RT2,RT3,RT4,RT5,RT6,RT7,RT8) 7.All RP(RN?) footprint change to 0402*4 8.P10 D6/D7/D8/D9/D13 -O for costdown 9.P21 Del COM,P16 Del RL_L,P23 Del wires with COM 10.P11 Add R94 avoid V_SA power oscillation 11.P12 Add R128, R138 avoid power oscillation 12.P25 Audio Line out cap(4 PCS) change to VPORT cap for avioding ESD 13.P22 EZ_Charge On 14.MC125,MC126 voltage change 10V-->16V 20111114

NOTE:

Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_0_8.pdf,
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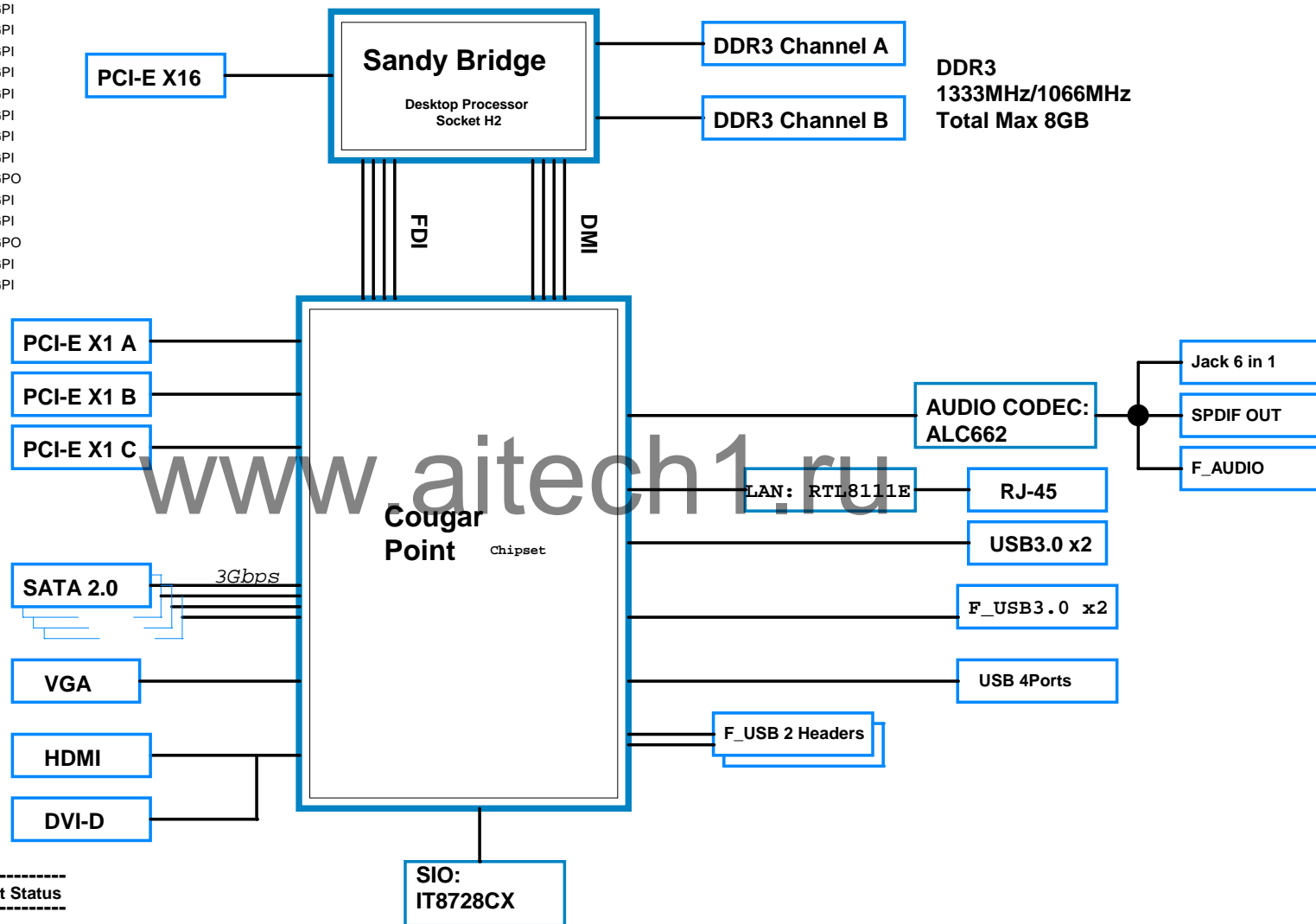


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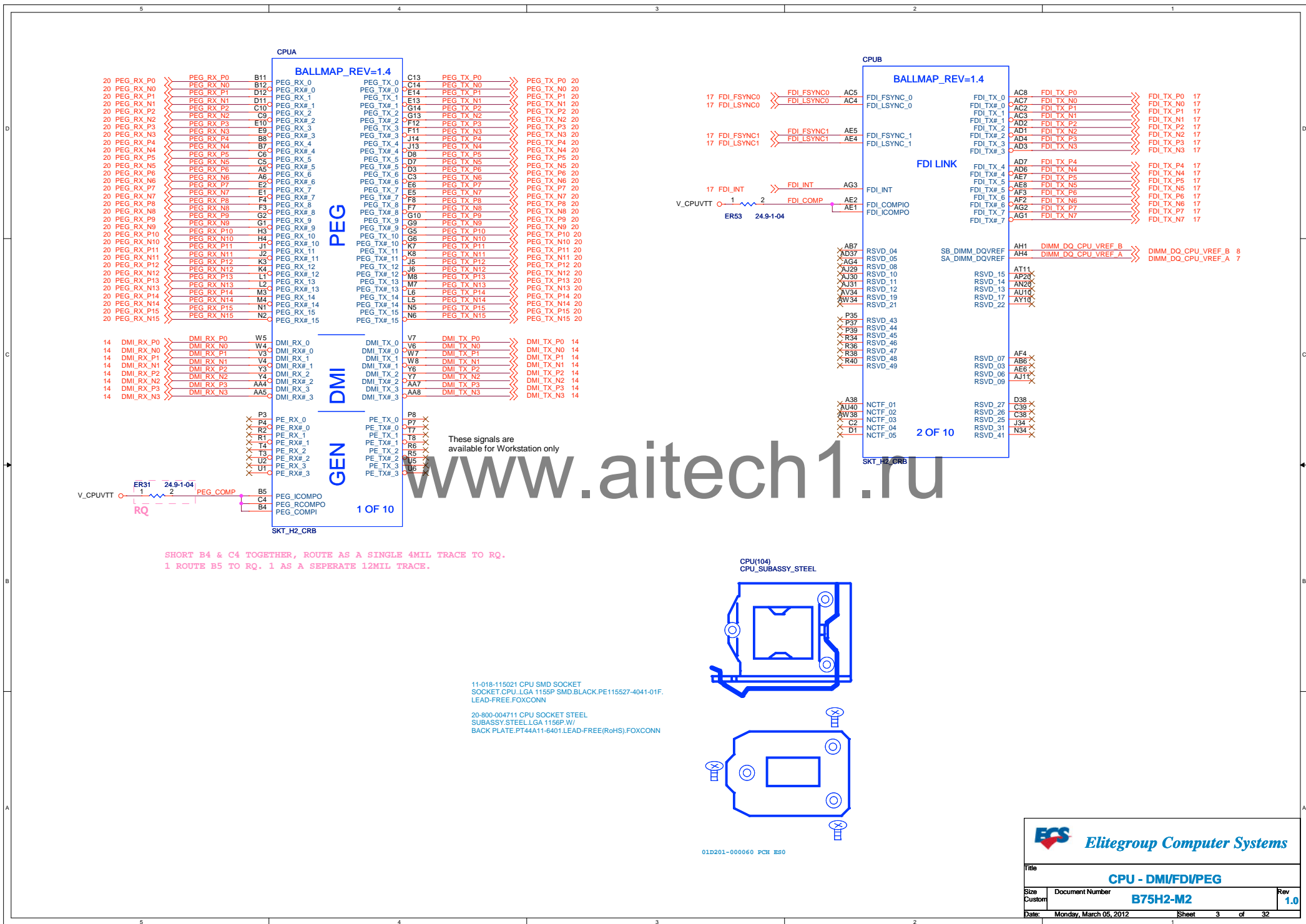
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



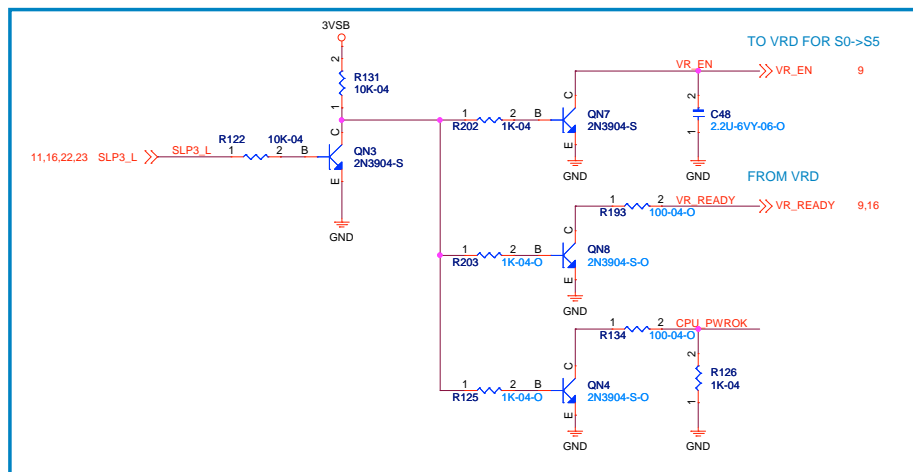
CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0] X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

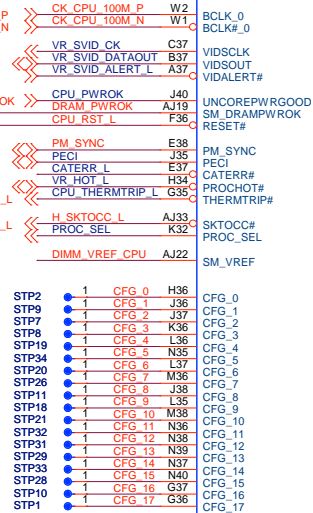
CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4

Power Down Sequencing Circuit



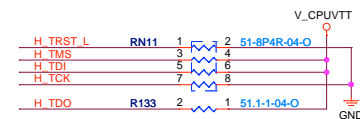
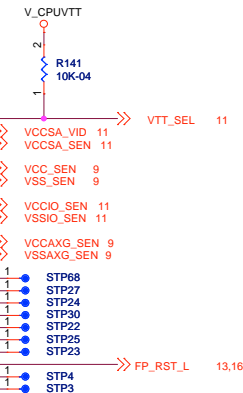
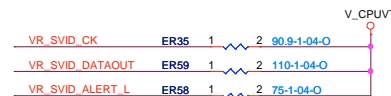
change test point for internal PU Jack05/25

BALLMAP_REV=1.4

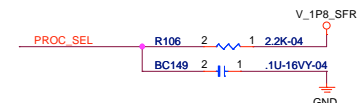
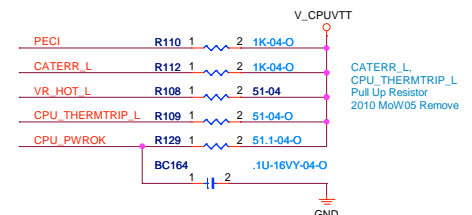


5 OF 10

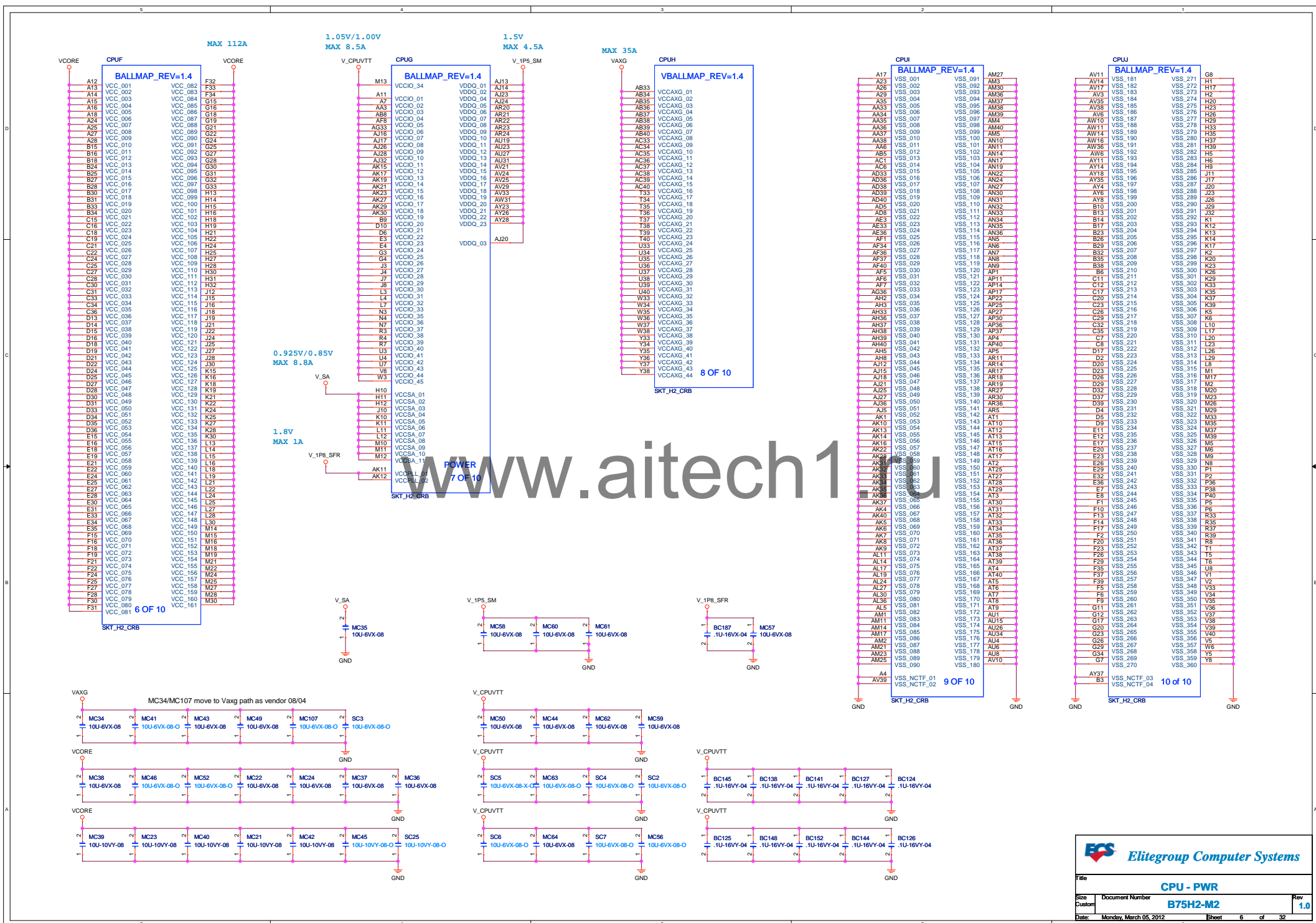
SKT_H2_CRB



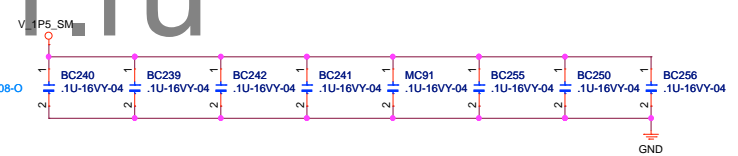
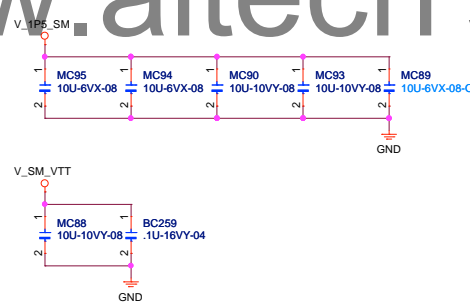
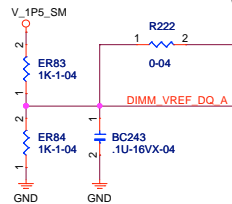
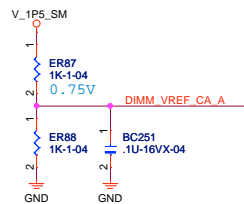
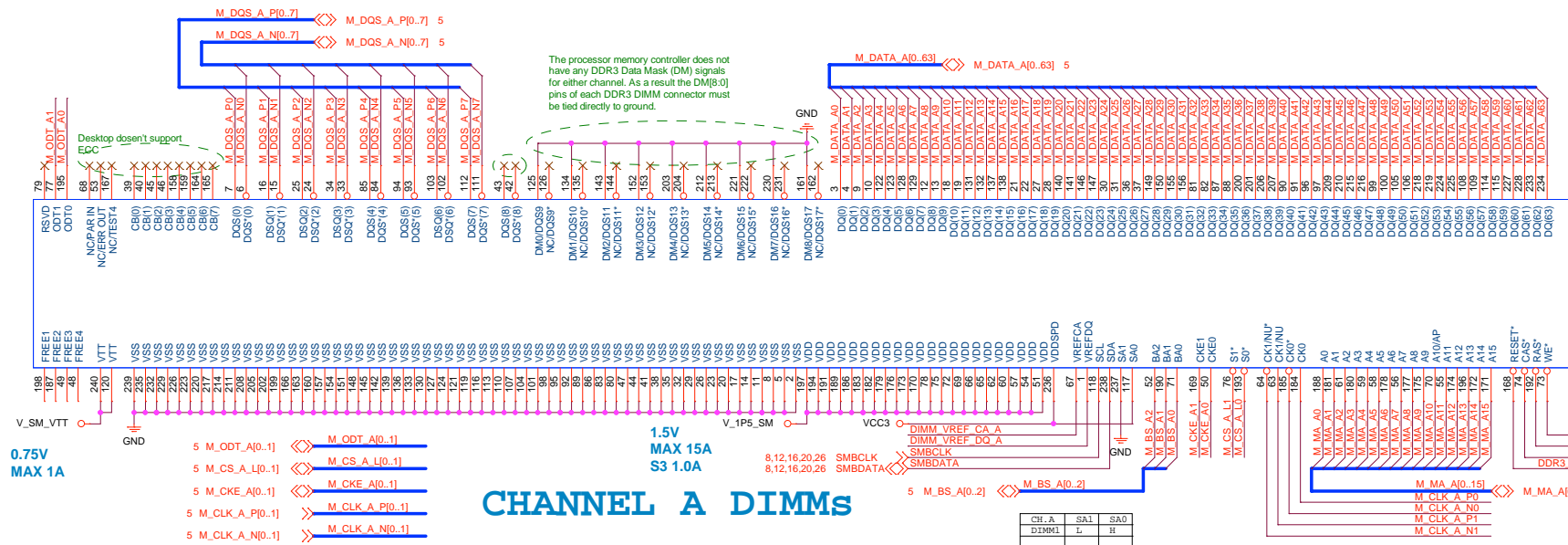
EDS P68/132 has internal PU Jack05/25



DMI/FDI termination voltage:
DC coupled: TX/RX to VCC IF sampled high
DC coupled: TX/RX to VSS IF sampled low
AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap



CHANNEL A DIMMs

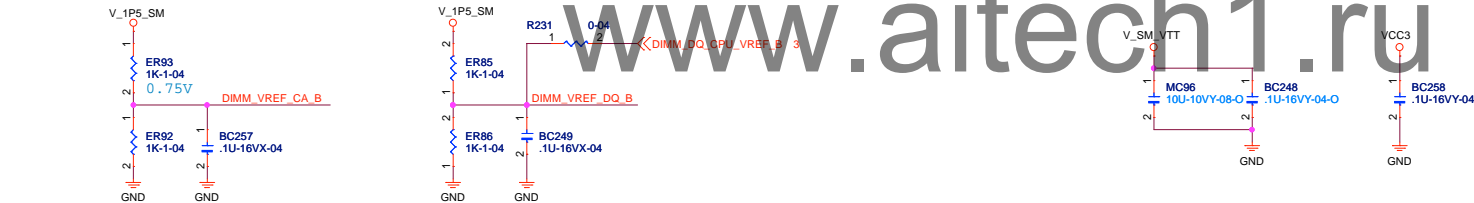


Del DIMM1 for always populate DIMM2 first Jack 05/13

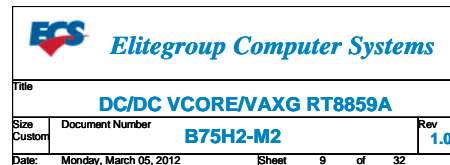
0.75V
MAX 1A

CHANNEL B DIMMs

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.



Del DIMM3 for always populate DIMM4 first Jack 05/13

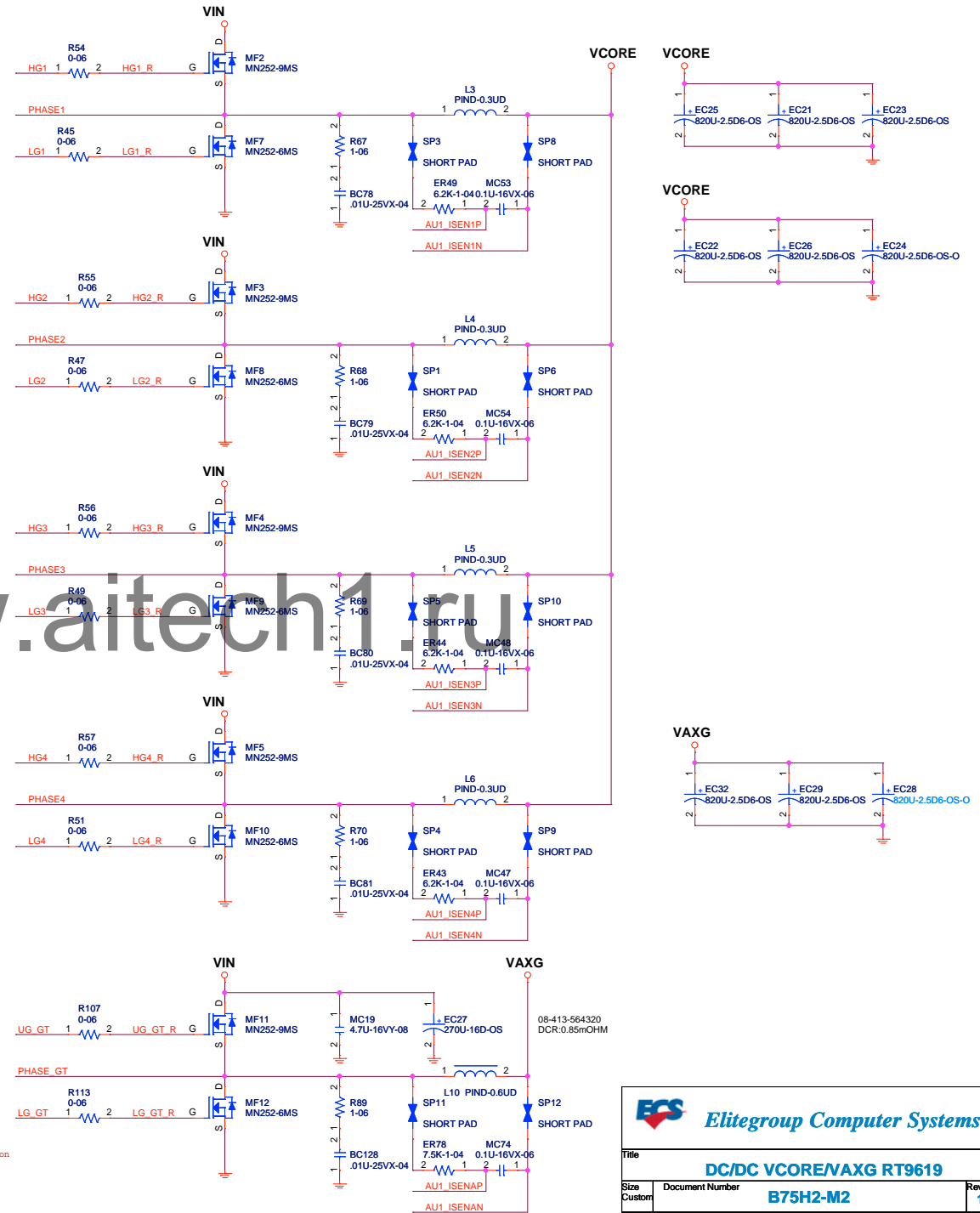
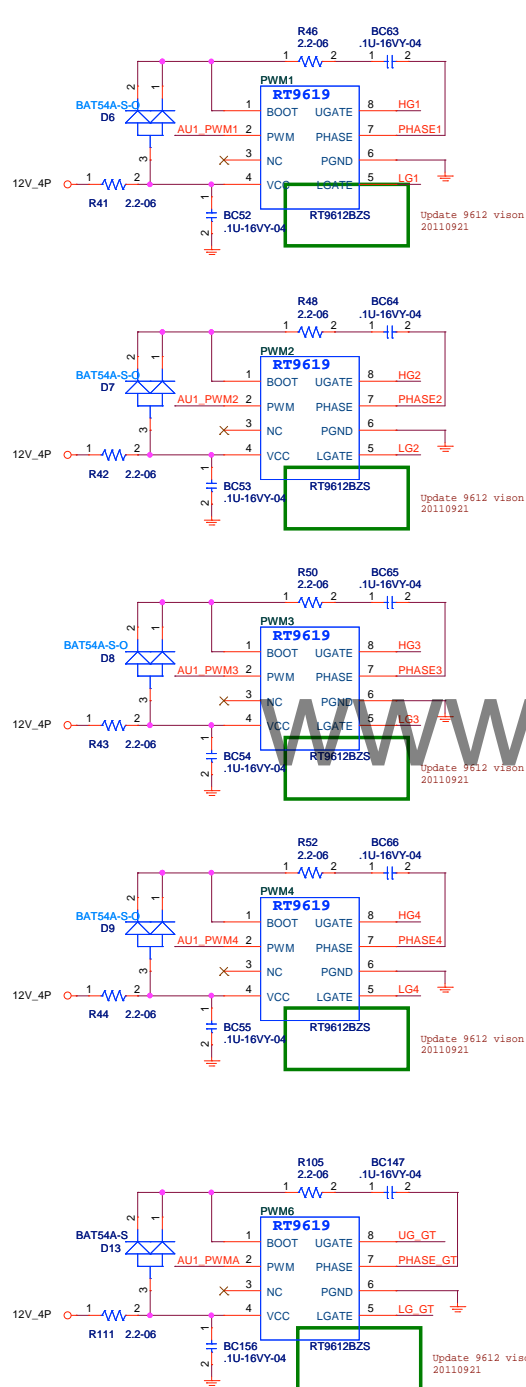


External Connection

VCC
VCCORE
12V_4P
VCC3
VIN

9 AU1_PWM[1..4] → AU1_PWM[1..4]
9 AU1_ISEN1P → AU1_ISEN1P
9 AU1_ISEN1N → AU1_ISEN1N
9 AU1_ISEN2P → AU1_ISEN2P
9 AU1_ISEN2N → AU1_ISEN2N
9 AU1_ISEN3P → AU1_ISEN3P
9 AU1_ISEN3N → AU1_ISEN3N
9 AU1_ISEN4P → AU1_ISEN4P
9 AU1_ISEN4N → AU1_ISEN4N
4,9 VCC_SEN → VCC_SEN
4,9 VSS_SEN → VSS_SEN

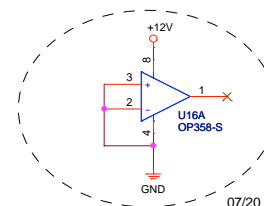
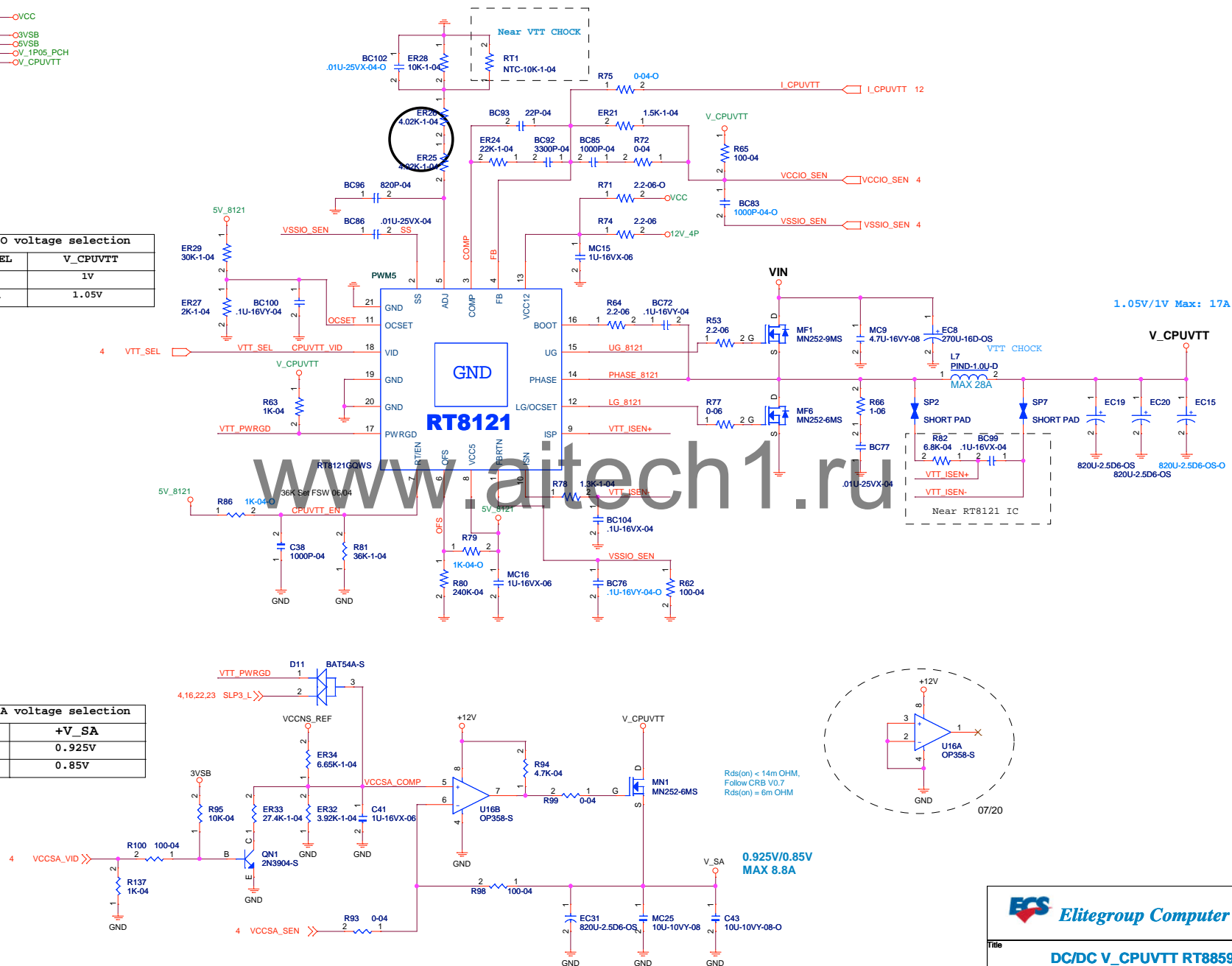
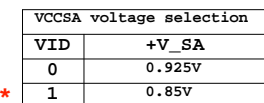
9 AU1_PWMA → AU1_PWMA
9 AU1_ISENAP → AU1_ISENAP
9 AU1_ISENAN → AU1_ISENAN
4,9 VCCAXG_SEN → VCCAXG_SEN
4,9 VSSAXG_SEN → VSSAXG_SEN



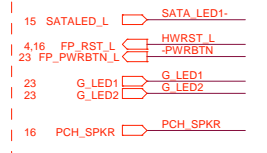
Pin connection diagram showing the following connections:

- VCC to VCC
- 3VSB to 3VSB
- 5VSB to 5VSB
- V_1P05_PCH to V_1P05_PCH
- V_CPUVTT to V_CPUVTT

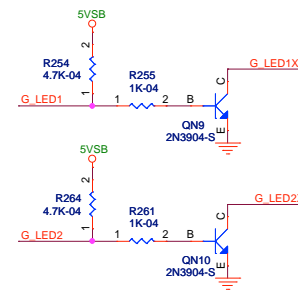
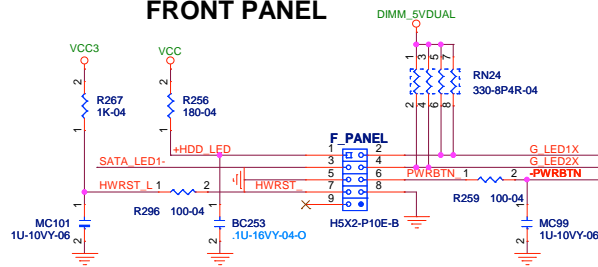
VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V



External Connection

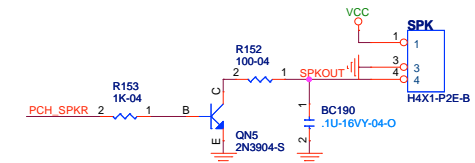


FRONT PANEL



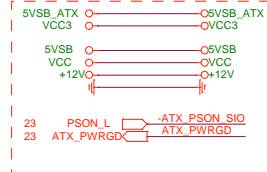
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
G_LED3	G	GB	YB	OFF	OFF

B: Blinking

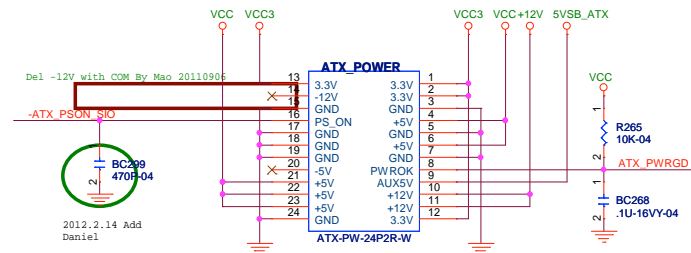


POWER CONNECTOR

External Connection



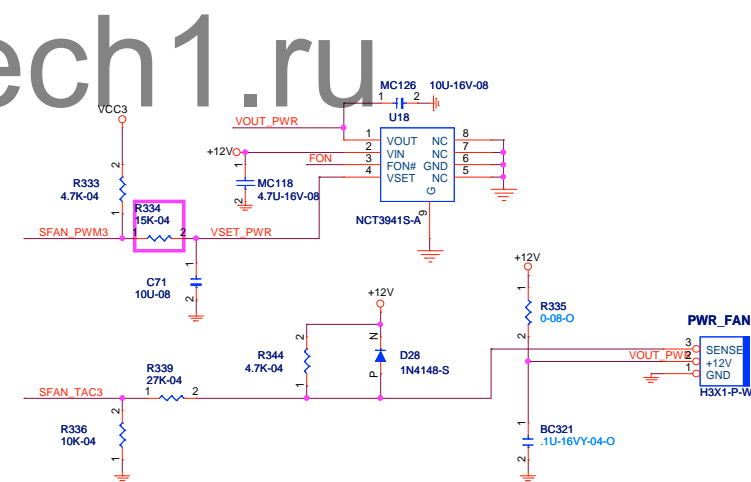
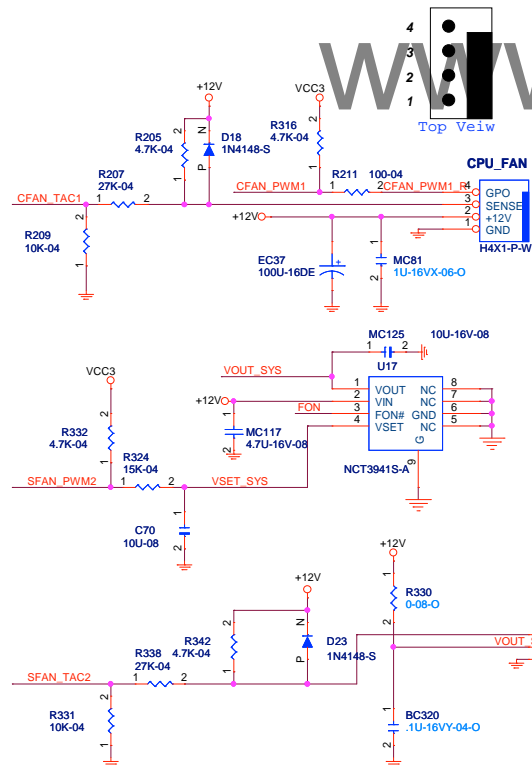
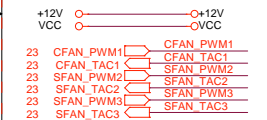
F_PANEL		
1	2	4
3	4	8
5	6	12
7	8	16
9	X	20



For EMI.

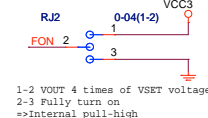
FAN

External Connection

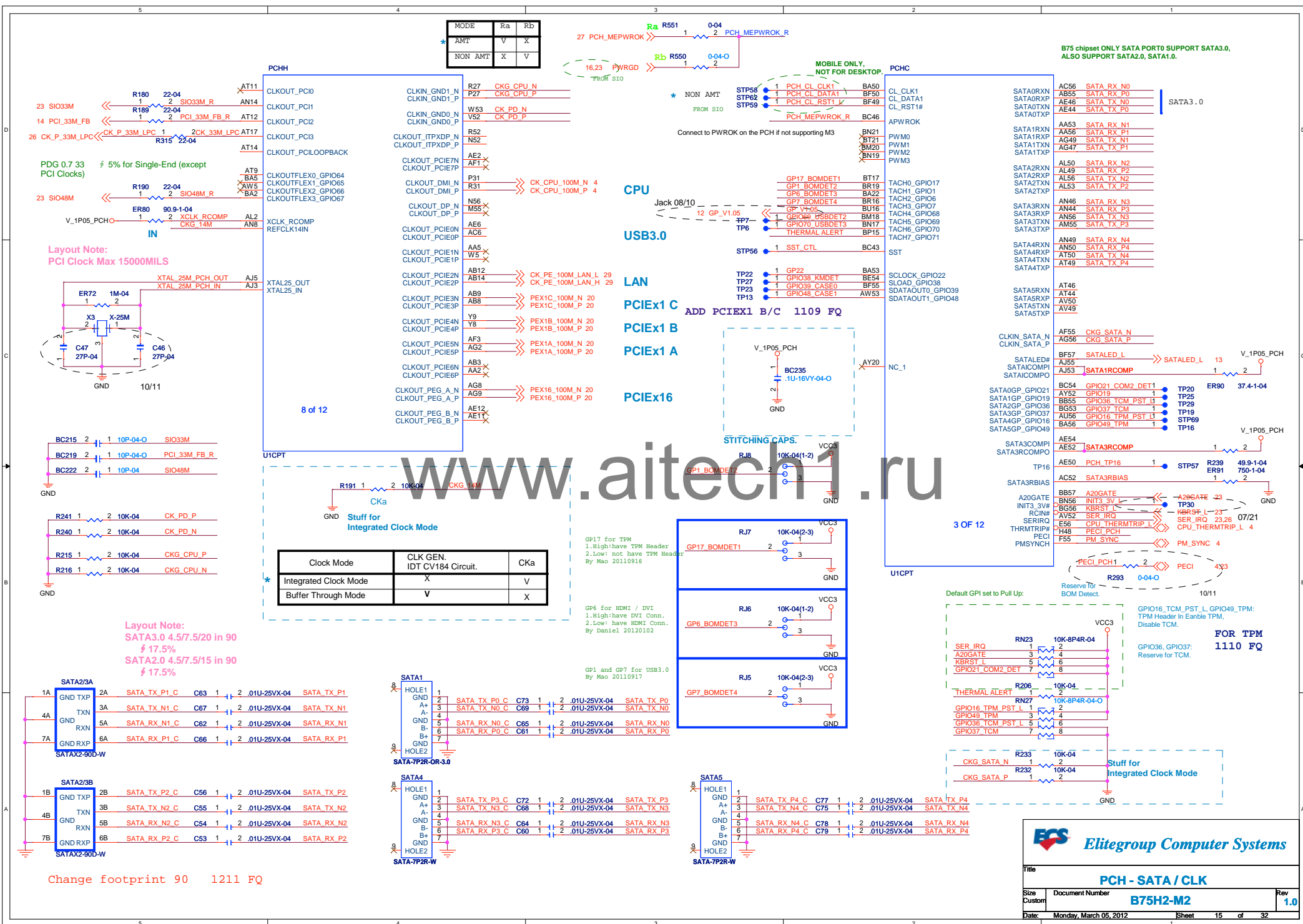


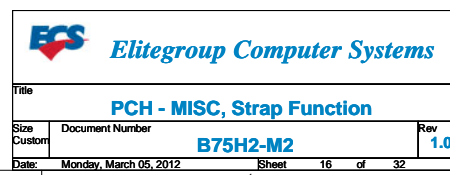
FQ 1217

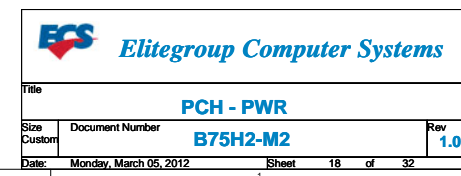
Add 3 pin control Fan

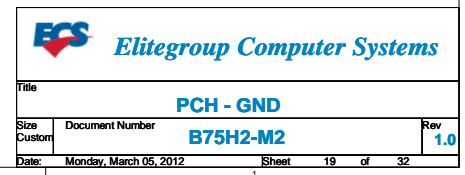


Front Panel,FAN,PowerConn	
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PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A

PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A

PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A

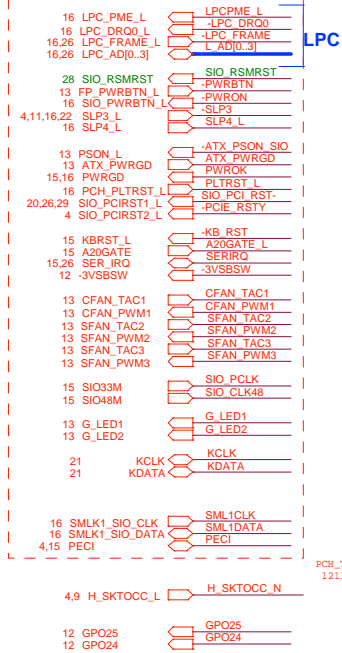
PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A

ADD PCIEx1 *2 1109 FQ

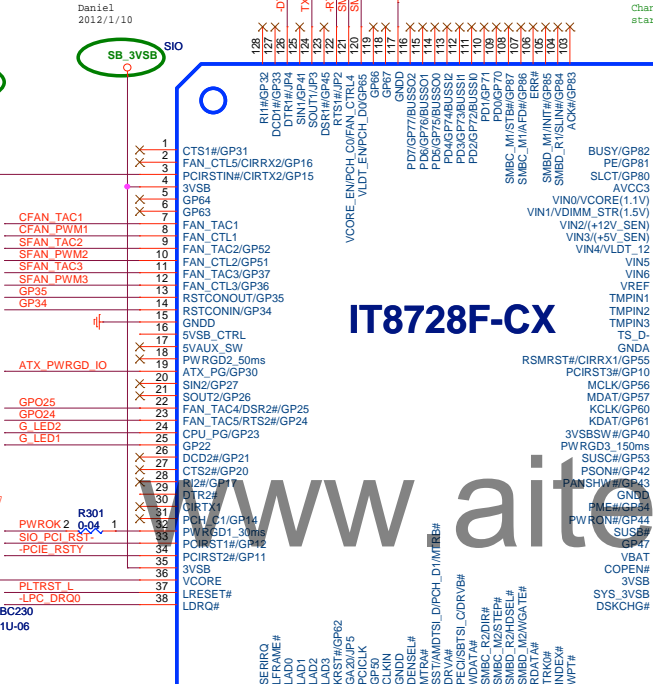
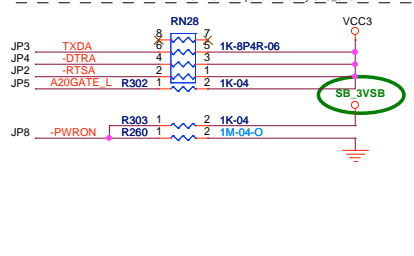
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Slot - PCI-EX16/PCI-EX1		
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PCI-E X1 A Decoupling Cap.

A pin-to-pin connection diagram for the 3VSB module. It shows two columns of pins. The left column pins are: 3VSB, 5VSB, VCC3, VBAT_IO_S, VCC, V_1P5_SM, V_CPUVTT, and VCORE. The right column pins are: 3VSB, 5VSB, VCC3, VBAT_IO_S, VCC, V_1P5_SM, V_CPUVTT, and VCORE. Each pin in the left column is connected to its corresponding pin in the right column by a horizontal line.

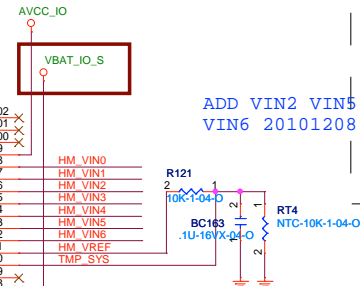


Pin	Signal	Value	Description
JP2 Pin122	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP4 Pin126	kPWR_EN	1	K3 power sequence function is enabled
		0	K3 power sequence function is disabled
JP3 Pin124	FAN_CTL_SEL	11	The default value of EC index 63b6B873h is 00h
JP5 Pin46		10	The default value of EC index 63b6B873h is 8Fh
		01	The default value of EC index 63b6B873h is 00h
		00	The default value of EC index 63b6B873h is 00h
JP8 Pin72	RSMRST_SEL	1	RSMRST# output detected by 3VSB
		0	RSMRST# output detected by SYS_3VSB

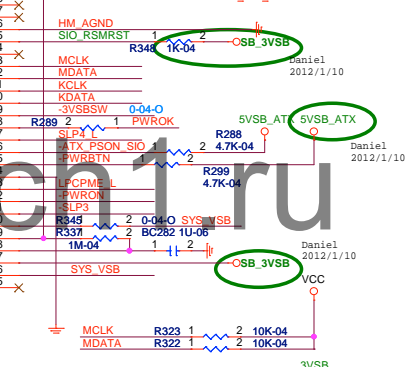


IT8728F-CX

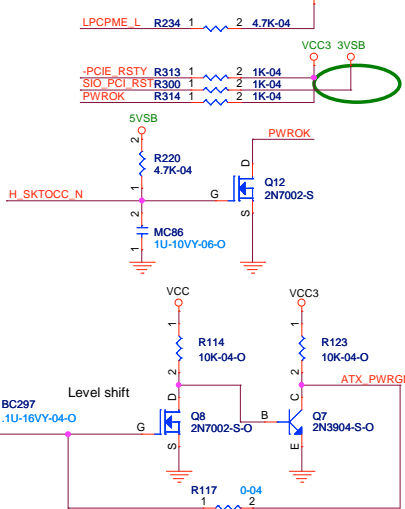
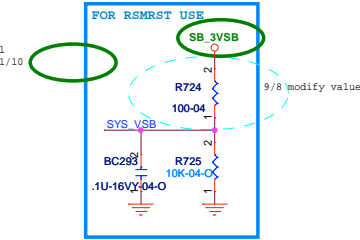
Change VBAT_IO to VBAT_IO_S for avoid
starting up after closing illegally By Mao 20110902




```
ADD VIN2 VIN5
VIN6 20101208 FQ
```

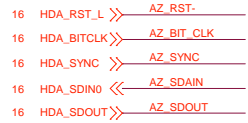
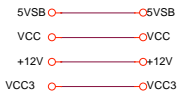
[illegible]

- * HM_VIN0 for VCORE
- * HM_VIN1 for V_DIMM
- * HM_VIN2 for +12V
- * HM_VIN3 for VCC
- * HM_VIN4 for CPUVTT
- * HM_VIN5 for VAXG
- * HM_VIN6 for V_1P05_PCH



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External Connection



* VCC1.5 can remove for non-Intel G4X platform

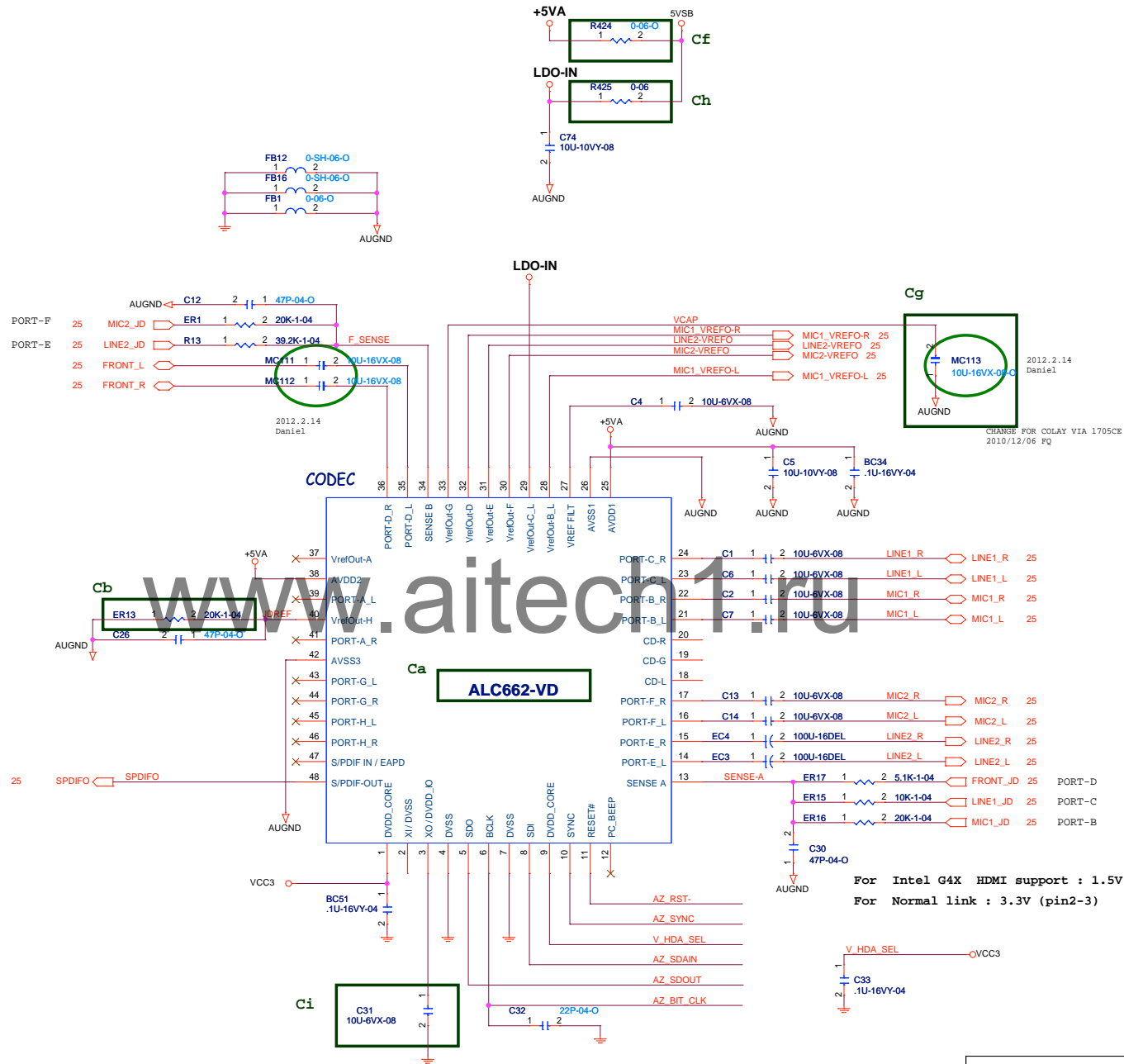
Pin Difference

Pin	ALC662 VD	VT1705CE
3	REG VREF	GPI01
4	GPI01	DVSS
25	LDO OUTPUT	LDO VIN
29	LDO VIN	OPTION CAP
33	LINE1 VREF	LDO OUTPUT
37	FRONT VREF ?	NC
38	LDO OUTPUT	LDO VIN
45	DMIC DATA	NC
46	DMIC CLK	NC

BOM Difference

Location	ALC662 VD	VT1705CE
Ca	ALC662-VD0-GR	VT1705CE
Cb	20K-1-04	5.1K-1-04
Cc	V	X
Cd	2.2K-04	3.3K-04
Ce	75-04	16-04
Cf	X	V
Cg	X	V
Ch	V	X
CI	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

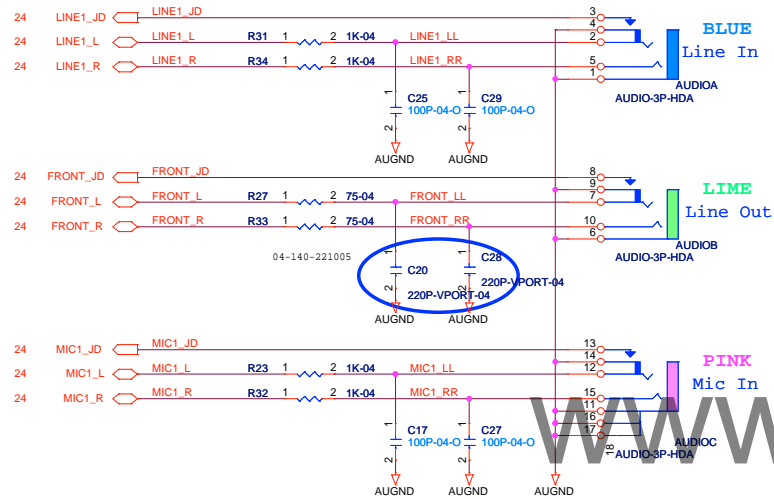


External Connection

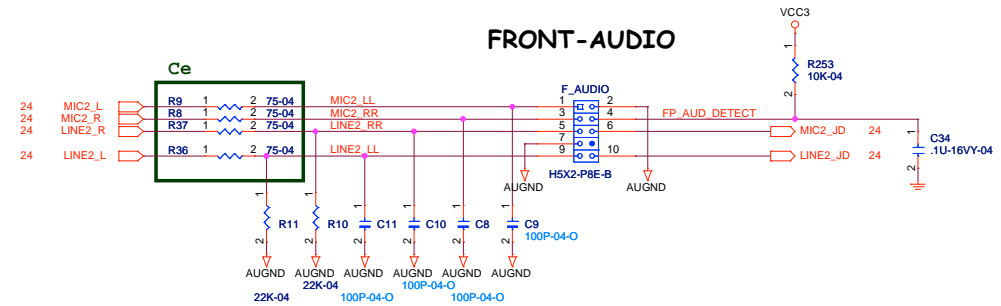
16 FP_AUD_DETECT << FP_AUD_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

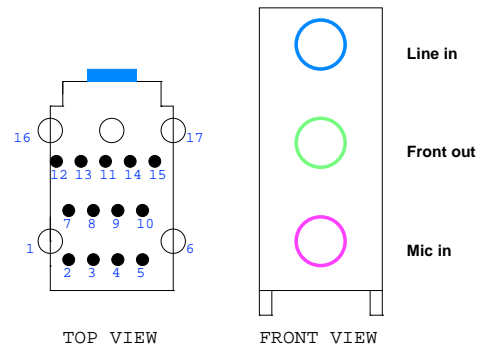
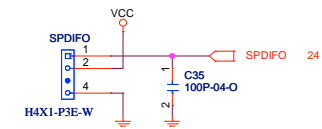
REAR-AUDIO Non re-tasking for rear panel



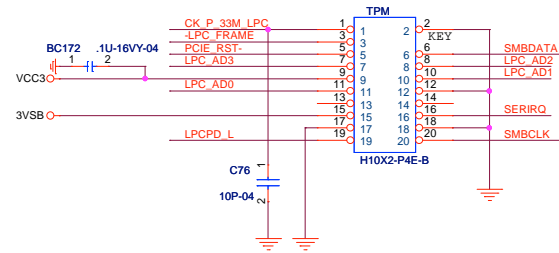
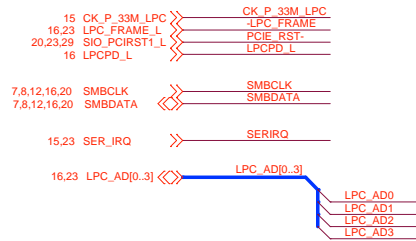
FRONT-AUDIO



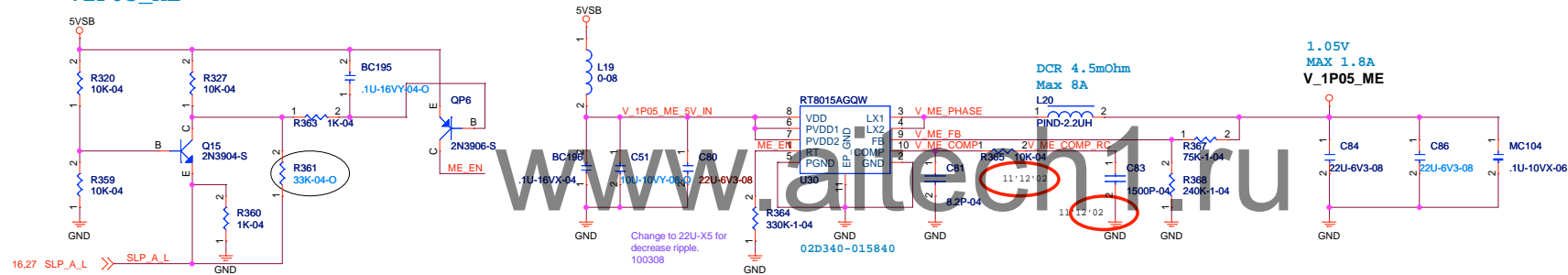
SPDIF-OUT



TPM HEADER



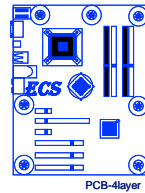
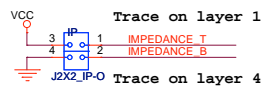
V1P05_ME



SLPAMT_L	EN	V_1P05_ME
High	5VSB	Enable
Low	0 V	Disable

1)Circuit type 1

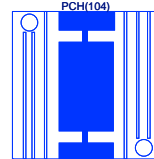
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Layer 2:PWR	<input type="text"/>
Layer 3:GND	<input type="text"/>
Layer 4:BOTTOM	<input type="text"/>



PCB STACK:

L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

JP-WI-P6.25



20-120-011476

5series PN:20-120-010851

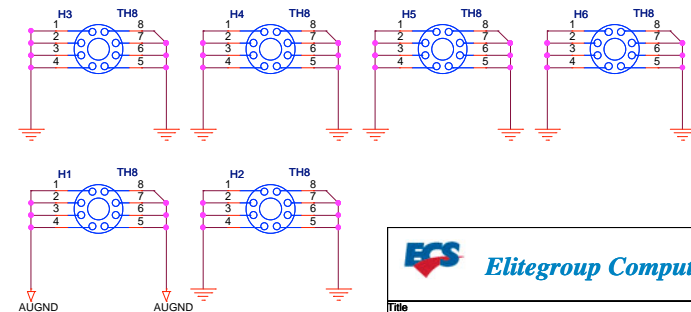
CLR_CMOS(1-2)



JP-R

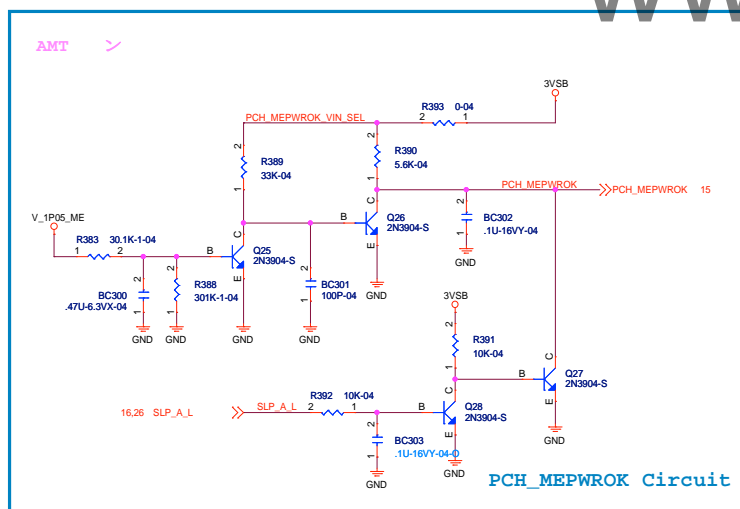
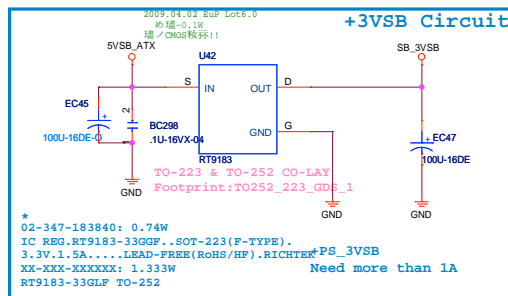
BT(104)
+
KTS
LITHIUM BATTERY
CD2032

CR2032



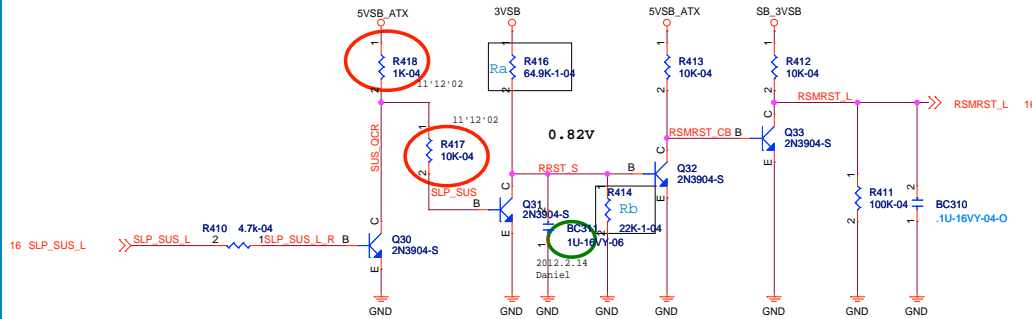
Elitegroup Computer Systems

Title			
TPM, GND, 104, V_1P05_ME			
Size Custom	Document Number		Rev
	B75H2-M2		1.0
Date:	Monday, March 05, 2012	Sheet	26 of 32

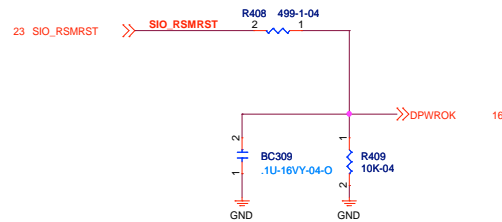


RSMRST Circuit

MODIFY Ra/Rb VALUE FOR FOLLOWING RULES
 1) AC ON: 3VSB vs RSMRST(t204: min 10ms)
 2) AC OFF: 3VSB > 2.9V when RSMRST < 0.8V



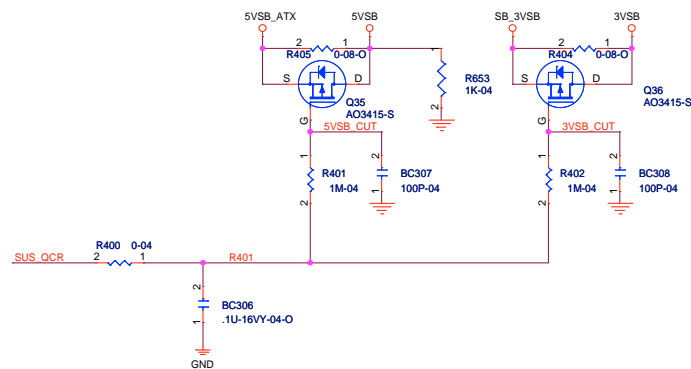
DPWROK Circuit



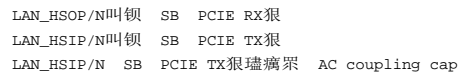
SUSACK_L CTRL CIRCUIT



SUS_3/5VSB SWITCH



Pin 1-20 connector diagram for the USB3.0 module. The diagram shows a 20-pin connector with pins numbered 1 to 20. Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19 are labeled with USB signals: USBVCC3, 3VSB, AUGND2, CK PE_100M_LAN_H, CK PE_100M_LAN_L, LAN_TX_P6, LAN_TX_N6, LAN_RX_P6, LAN_RX_N6, USB_N10, USB_P10, USB_N11, USB_P11. Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20 are labeled with PCIe signals: OUSBVCC3, C8VSB, AUGND2, PCIE_WAKE_UP, PCIE_LAN1_RST, CK LAN1_H, CK LAN1_L, LAN1_HS1P, LAN1_HSN1, LAN1_HSOP, LAN1_HSON. Pins 16, 17, 18, 19 are labeled with PCIE signals: 16,20 PCIE_WAKE_L, 20,23,26 SIO_PCIRST1_L.



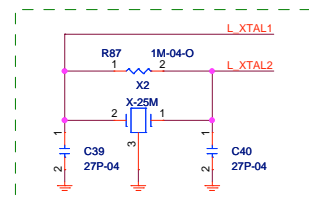
The image shows a detailed PCB layout for a LAN module. The central component is the LAN1 chip, which is a LAN8710E-VL-CG. The layout includes various components and their values, as well as a large watermark 'www.aitech1.ru'.

Components and Values:

- ER30: 1 2.49K-1-04
- LAN1_RSET
- L_XTAL2
- L_XTAL1
- LAN1_ACTIVE
- GPO1
- EESKLINK1
- R84: 1 1K-04
- BC94: 1 2 10-16VY-04
- MC18: 1 2 10U-6VX-08
- IND-47U-S: 1 2 0-06
- R76: 1 2 10K-04
- R73: 1 2 10K-04
- R58: 1 2 1K-04
- R61: 1 2 15K-04
- R60: 1 2 10K-04
- R59: 1 2 10K-04
- C37: 1 2 .1U-16VX-04
- C36: 1 2 .1U-16VX-04
- C292: 1 2 10U-16VY-04-0
- BC276: 1 2 10U-16VY-04-0
- BC277: 1 2 10U-16VY-04-0

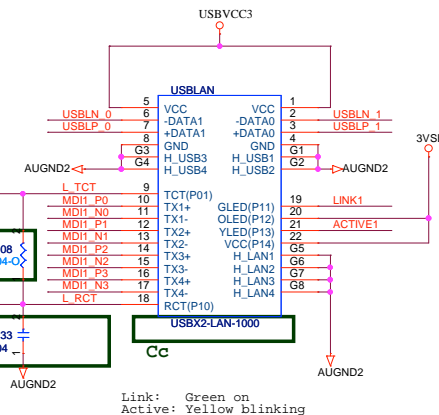
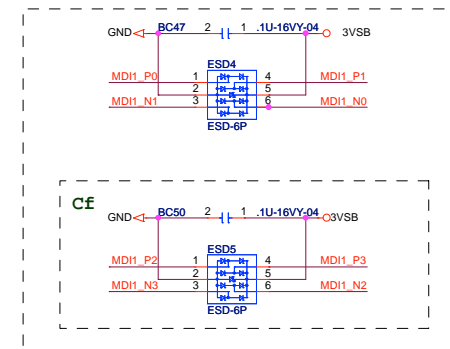
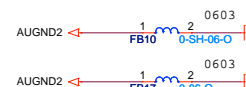
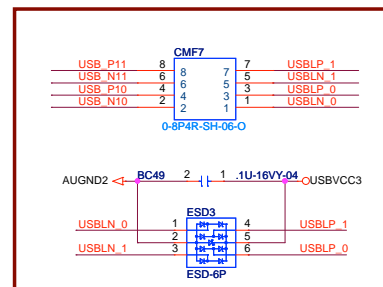
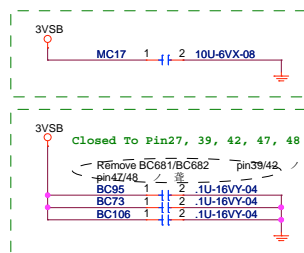
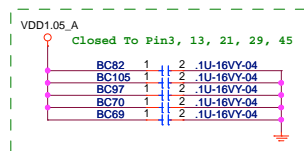
Labels and Connections:

- VDD1.05_A
- 3VSB
- LAN
- GND
- MDI0_P0
- MDI0_N0
- MDI0_P1
- MDI0_N1
- MDI0_P2
- MDI0_N2
- MDI0_P3
- MDI0_N3
- MDI0_P4
- MDI0_N4
- MDI0_P5
- MDI0_N5
- MDI0_P6
- MDI0_N6
- MDI0_P7
- MDI0_N7
- MDI0_P8
- MDI0_N8
- MDI0_P9
- MDI0_N9
- MDI0_P10
- MDI0_N10
- MDI0_P11
- MDI0_N11
- MDI0_P12
- MDI0_N12
- MDI0_P13
- MDI0_N13
- MDI0_P14
- MDI0_N14
- MDI0_P15
- MDI0_N15
- MDI0_P16
- MDI0_N16
- MDI0_P17
- MDI0_N17
- MDI0_P18
- MDI0_N18
- MDI0_P19
- MDI0_N19
- MDI0_P20
- MDI0_N20
- MDI0_P21
- MDI0_N21
- MDI0_P22
- MDI0_N22
- MDI0_P23
- MDI0_N23
- MDI0_P24
- MDI0_N24
- MDI0_P25
- MDI0_N25
- MDI0_P26
- MDI0_N26
- MDI0_P27
- MDI0_N27
- MDI0_P28
- MDI0_N28
- MDI0_P29
- MDI0_N29
- MDI0_P30
- MDI0_N30
- MDI0_P31
- MDI0_N31
- MDI0_P32
- MDI0_N32
- MDI0_P33
- MDI0_N33
- MDI0_P34
- MDI0_N34
- MDI0_P35
- MDI0_N35
- MDI0_P36
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- MDI0_N102
- MDI0_P103
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- MDI0_N140
- MDI0_P141
- MDI0_N141
- MDI0_P142</



The image contains two circuit diagrams, each enclosed in a dashed green rectangular border. The top diagram is for the VDD1.05_A pin. It shows a red wire connected to the pin, with a green text label "Closed To Pin6,9,41" above it. Below the pin, a purple wire branches out to two capacitors. The first capacitor is labeled "BC84 1" and the second is labeled "BC91 1". Both capacitors are connected to a common ground symbol on the right, which is labeled "2 .1U-16V-Y-04". The bottom diagram is for the 3VSB pin. It shows a red wire connected to the pin, with a green text label "Closed To Pin12" above it. Below the pin, a purple wire branches out to a single capacitor labeled "BC74 1". This capacitor is connected to a common ground symbol on the right, which is labeled "2 .1U-16V-Y-04".

	RTL8111E-VL 1000M	RTL8105E-VL 10/100M
Ca	RTL8111E-VB-GR	RTL8105E-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-25VX-04
Cf	V	X
Cg		



ATX P/S WITH 1A STBY CURRENT					
5VSB	5V	3.3V	12V	-12V	
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	

ATX4P
12V
+/-5%

Switching RT8859A 4 phases

Vcore:0.65~1.3V 112Amax

Switching RT8121 1 phase

Vaxg:0.65~1.3V 35Amax

Switching RT8105

V_CPU_VTT:1.05V 17Amax

DDR3 DIMM (4) 1333MHz	
VDDQ	15A_S0
V_SM_VTT	1.0A_S0

V_DIMM:1.5V 28.5Amax

LDO APL5336

DDR_VTT:0.75V

Linear OP358

PCH_CORE:1.05V 6.2Amax

Intel Sandy Bridge CPU			
VCCP	VID	0.25~1.52V	85A(95W)
VAXG	VID	0.25~1.52V	25A
VTT		1.05V(1V)	8.5A
VCC_SA		0.925V(0.85V)	8.8A
VCCPLL		1.8V	1A
VDDQ		1.5V	4.5A

Intel Cougar Point (TDP 5.5W)			
V_PROC_IO	1.05V	1mA	
VccDMI	1.05V	0.057A	
VccCORE	1.05V	1.6A	
VccIO	1.05V	4.07A	
VccADPLLA	1.05V	0.1A	
VccADPLLB	1.05V	0.1A	
VccCLKDMI	1.05V	0.02A	
VccSSC	1.05V	0.105A	
VccDIFFCLKN	1.05V	0.055A	
VccASW(ME)	1.05V	1.61A	
VccDFTERM	1.8V	0.2A	
VccVRM	1.8V	0.159A	
Vcc3_3	3.3V	0.409A	
VccADRC	3.3V	0.068A	
VccSPI	3.3V	0.02A	
VccDSW3_3	3.3V	0.003A	
VccSUS3_3	3.3V	0.097A	
VccSUSHDA	3.3V	0.01A	
VccRTC	3.3V	6uA(G3)	
V5REF	5V	1mA	
V5REF_SUS	5V	1mA	

Fans
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x 2

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

Battery
3V

NEC_D720200		
VDD3P3	3.3V	TBD
VDD1P05	1V	TBD
CTRL1P0 internal LVR Output		

SUPER I/O IT8728		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
BAT 3.3V	3.3V	TBD

AUDIO ALC892		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

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Non AMT:
VccASW(ME) short to V1P05_PCH

V_ME:1.05V 1.8Amax

Linear LM324

V_S5B:1.8V 1.6Amax

Not support DSW mode:
VccDSW short to 3VSB

Extrenal from V1P05_PCH

3VDUAL P/N MOS

5VDUAL Switch IC UP7536

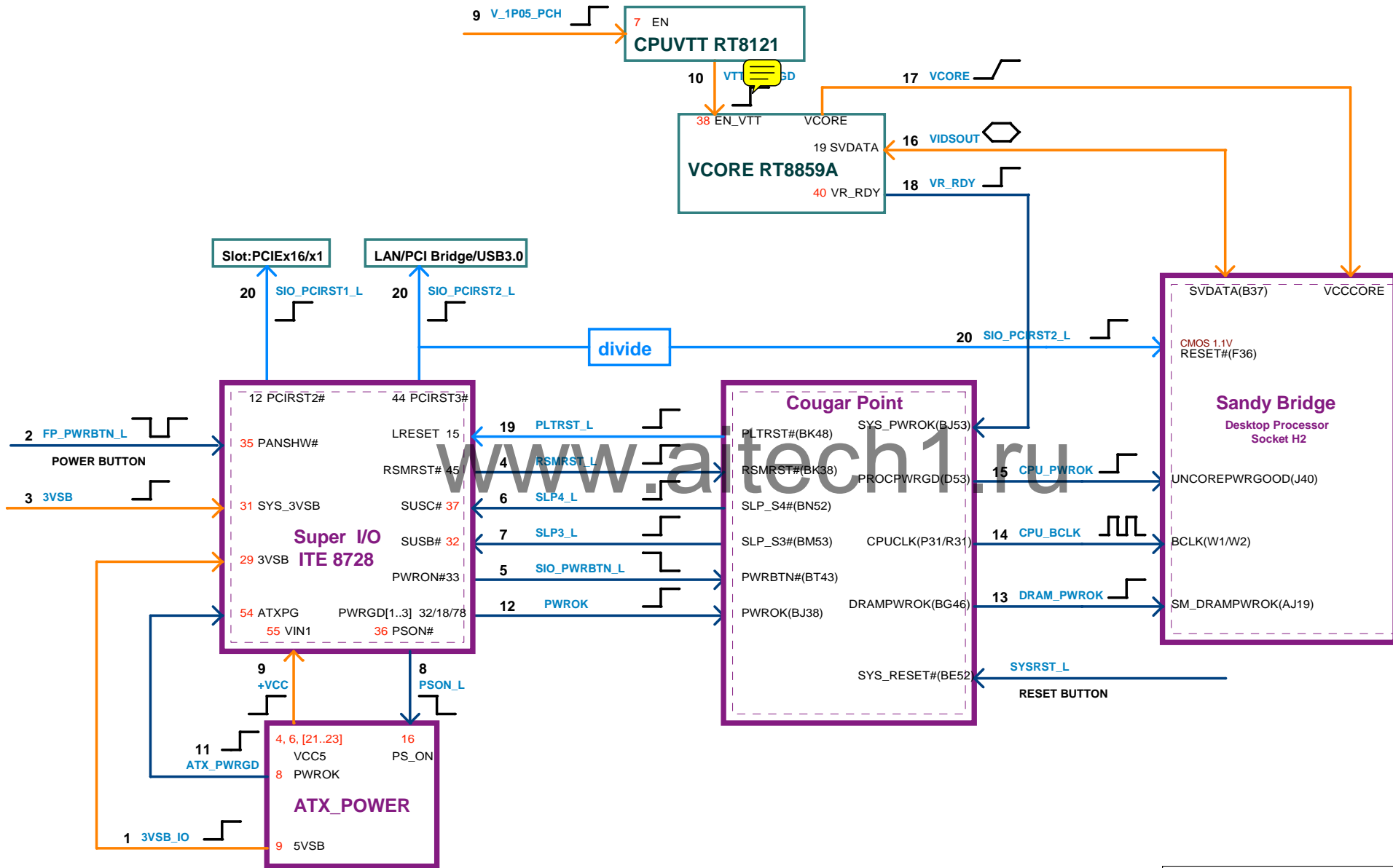
USB X4 Header	USB X4 IO	USB3.0
VDD	VDD	5VDual
5VDual	5VDual	2A
2.0A	2.0A	

X16 PCIe Slot per	X1 PCIe Slot per *3
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

Total 1 Slot

Total 2 Slots

Total 1 Slot



NOTE:

Sugar Bay Platform has two clock mode:

1. Integrated Clock Mode (Generate by PCH)

2. Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

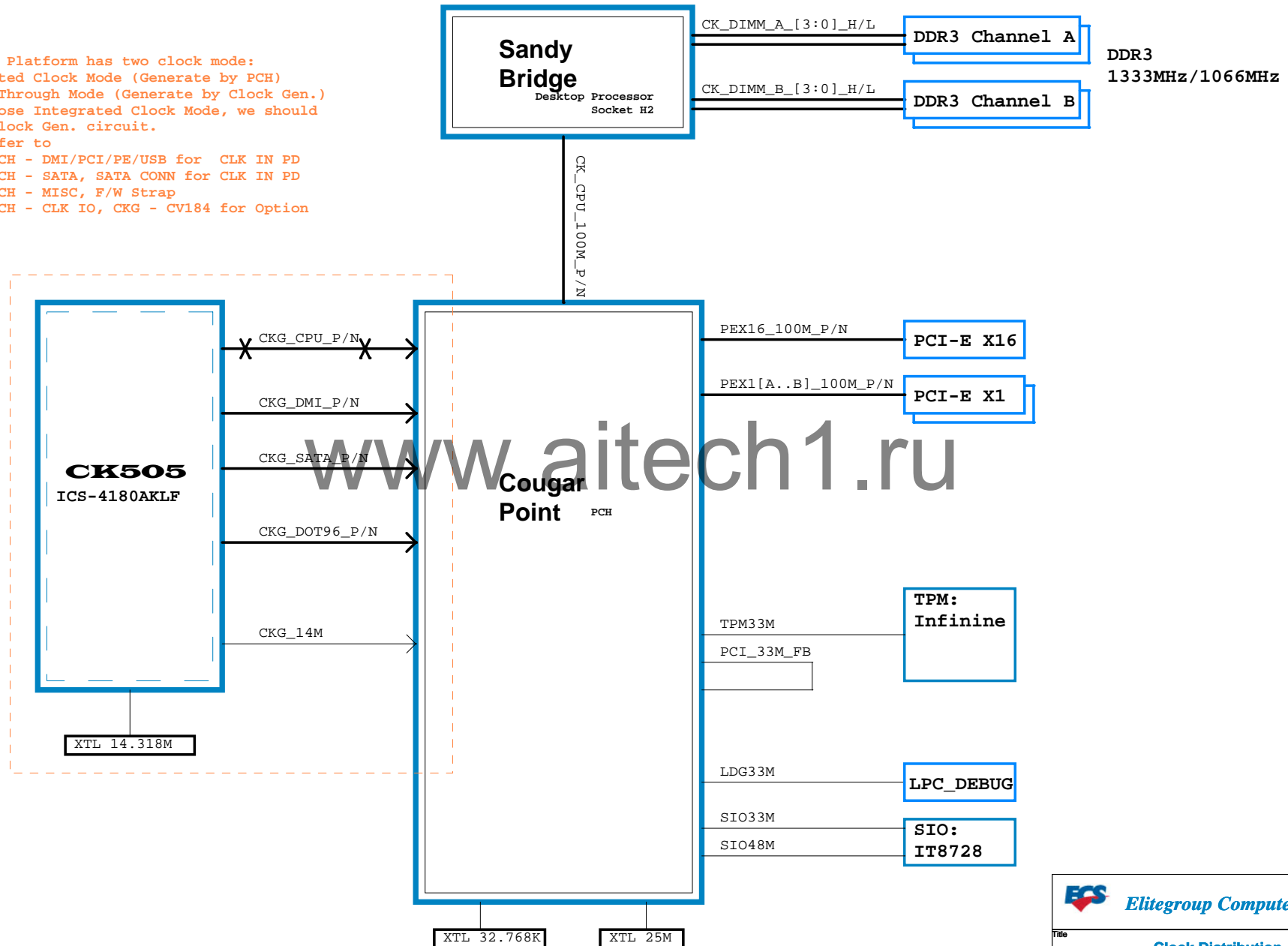
Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option



Elitegroup Computer Systems

Title
Clock Distribution

Size Custom Document Number
B75H2-M2

Rev
1.0

Date: Monday, March 05, 2012 Sheet 32 of 32